

CLAIMS

What is claimed is:

1. A method of fabricating an integrated circuit, comprising:

forming metal lines in a last metal level; and

5 depositing a low-k dielectric at least between the metal lines.
2. The method of claim 1 wherein the metal lines have a thickness that is at least about 8000 Angstroms.
3. The method of claim 1 wherein the metal lines have a thickness less than about 8000 Angstroms.
- 10 4. The method of claim 1 wherein the metal lines have a thickness that is at least about 12000 Angstroms.
5. The method of claim 1 wherein the metal lines have a thickness less than about 12000 Angstroms.
6. The method of claim 1 wherein the low-k dielectric has a dielectric
15 constant less than about 3.9.
7. The method of claim 1 wherein the metal lines are formed over a dielectric level that comprises a dielectric having a dielectric constant less than about 3.9.
8. The method of claim 1 wherein the low-k dielectric substantially fills a space between the metal lines.
- 20 9. The method of claim 1 wherein the metal lines comprise aluminum.
10. The method of claim 1 further comprising:

depositing a dielectric over the low-k dielectric; and

depositing a topside material over the dielectric.

11. The method of claim 10 wherein the dielectric comprises silicon dioxide.

12. The method claim 10 wherein the topside material comprises silicon

5 nitride.

13. A structure in an integrated circuit, the structure comprising:

a last metal level; and

a passivation level comprising a low-k dielectric at least between metal
lines in the last metal level.

10 14. The structure of claim 13 wherein the low-k dielectric substantially fills a
space between the metal lines.

15. The structure of claim 13 wherein the passivation level further comprises a
layer of dielectric over the low-k dielectric and a topside material over the layer of
dielectric.

15 16. The structure of claim 13 wherein the low-k dielectric has a dielectric
constant less than about 3.9.

17. The structure of claim 13 wherein the metal has a thickness between
about 8000 Angstroms and about 15000 Angstroms.

18. A structure in an integrated circuit, the structure comprising:

20 means for carrying a signal in a last metal level; and

means for reducing propagation delay of the signal, the means for
reducing propagation delay of the signal comprising a low-k dielectric.

19. The structure of claim 18 wherein the means for carrying the signal
comprises a metal line having a thickness between about 8000 Angstroms and about
5 15000 Angstroms.

20. The structure of claim 18 wherein the means for reducing propagation
delay of the signal comprises a low-k dielectric that substantially fills a space between a
metal line and an adjacent metal line in the last metal level.

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